

<b>Notice of References Cited</b>	Application/Control No. 09/768,911		Applicant(s)/Patent Under Reexamination CHOW ET AL.	
	Examiner David A. Zarneke		Art Unit 2827	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

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*	N	JP 61-147551	07-1986	Japan	Kano	
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wolf, Silicon Processing for the VLSI Era-Volume 2:Process Integration, Lattice Press, 1990, pp. 194-199, 387, 482 and 508
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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